Datasheet

5.4” Iridis® Display module

5.4", 130 ppi, 680 x 155 pixels, 7 colors

Part-No. 700050

Type D054_T2.1

Revision 1

17-May-2021

Revision Status	Date	Author	Reason of Modification
1	17-May-2021	RP	Initial Version derived from #700313, w/o temperature & update modes

Inhaltsverzeichnis

1. Introduction

1.1 Purpose of this document

This document describes the technical specification of the 5.4” Plastic Logic display module (680x155px), part number 700050. It defines general characteristics of the display module and the technical information required to integrate the display module into a product.

1.2 Key features of display module

- Electrophoretic display with integrated EPD controller & source driver IC on COF bonded at one short side and a gate driver IC on the other short side of that display
- Organic TFT active matrix backplane
- 680 x 155 pixels @ 130 ppi
- AceP (Advanced color e-Paper) seven colors with red, blue, green, yellow, orange, cyan, magenta plus black and white
- Incorporates industry-leading bi-stable electrophoretic display technology
- Ultra-wide viewing angle
- Enables robust product design
- Flexible stack enabling curved product integration
- Glass free

1.3 Display variants

The display can be manufactured with different media for various applications. Depending on the media, the thickness of the display module can vary, the lateral dimensions will be the same.

Display Type	Display Colors	P/N	Comments
Lectum®	16 Greylevels	700313	
Iridis®	7 colors plus black and white	700050	

1.4 Handling requirements

The display module is an electrostatic discharge (ESD) sensitive device. Ensure proper ESD precautions are in place to avoid damage to the display module.

Take appropriate care to protect the rear side of the display module from indents and punctures as this may damage the display. Take appropriate care to ensure the minimum bend radii of the flex tails are not violated (see Table 1).

In the application the gate and source driver chips must be protected from light to avoid unwanted drift effects.

The area of the driver chips must not be bent.

1.5 General parameters

Parameter	Value	Unit	Comments
Module dimensions folded	153.84 x 35.0	mm	With COFs folded
Module thickness	0.545±0.04	mm	Active area w/o Liners
Active screen dimensions	133.28 x 30.38	mm	Equivalent to 5.4” diagonal
Active screen resolution	680 x 155	pixels	
Pixel pitch	196 x 196	µm	Equivalent to 130ppi.
Top Surface finish hard coat	2	H	Antiglare, UV-protection
Driver Chip Source	1	piece	Epson S1D13541 with build in EPD controller (on COF)
Driver Chip Gate	1	piece	UC8434 (on COF)
COF minimum internal bend radius	0.4	mm	Bend not permitted at IC location.

Table 1: general specification

2. Mechanical specification

2.1 Outline dimensions

Please request technical drawing document for full details. Plastic Logic is providing a display module consisting of the actual flexible display.

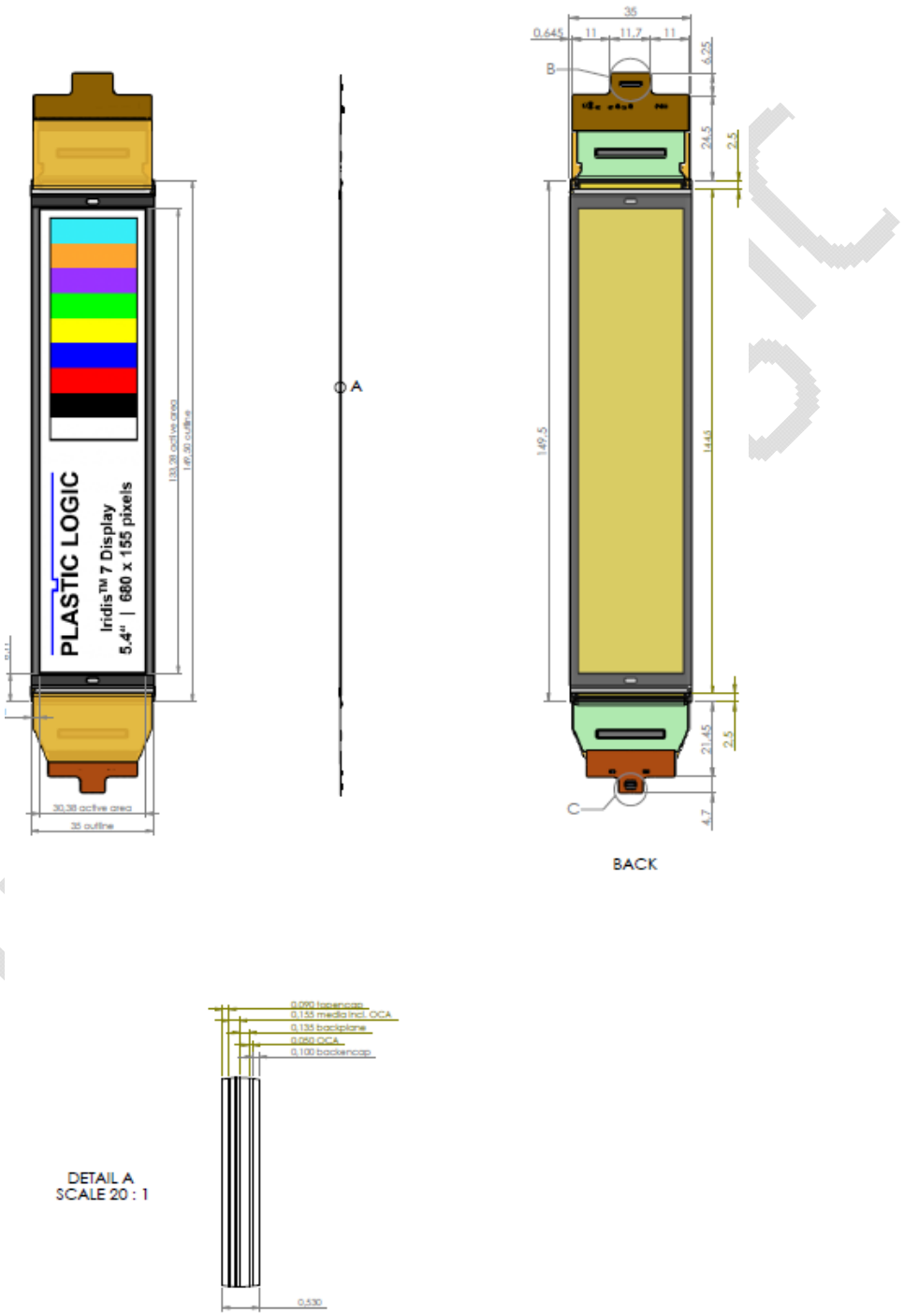


Figure 1: Outline dimension

3. Optical specification

3.1 Optical requirements

Specific display grey levels are defined using the terminology GLx, where x = 0-15. GL0 corresponds to "black" and GL15 corresponds to "white".

Grey levels and colors are measured using the L* scale, which is the lightness component of the CIE 1976 CIELUV and CIELAB [2] colour spaces. Measurements in L* can be related to reflectivity using the formula $L^*=116(L/L_w)^{1/3}-16$, where L and Lw are measured in % reflectance and Lw is defined as 100%. This formula is valid for L* > 8.

The following table lists the criteria for the optical inspection of the display module. Inspection shall be done after an image updates with the display specific settings as provided by Plastic Logic (waveform, VCOM, …).

- Viewing Angle : α =±45°
- Viewing Distance : 30cm±10cm
- Ambient Luminance : 700~1000 Lux
- Ambient Temperature : 20°C~25°C
- Ambient Humidity : 40~70%rH

Parameter	Description	Min	Max	Unit
White state	Median white	65	-	L*
Black to White difference	(Median white) – (Median black)	38	-	L*
Pixel Yield		>99.99%		

Table 2: Optical requirements

4. Electrical specification

4.1 Connector

Recommended type of connector:

- 26ways, WP7A-S026VA1-R8000, mezannine connector
- 10ways, WP7A-S010VA1-R8000, mezannine connector

Electrical pin-out

Pin number	Symbol	Function
1	CLKI	EPDC clock
2	HIRQ	Interrupt line from EPDC; optional: if not used keep open
3	VSNEG	Negative HV supply for source driver (-15V typ)
4	VCC_3V3	3V3 power pin
5	VSPOS	Positive HV supply for source driver (+15V typ)
6	SPICLK	SPI clock for EPDC host interface
7	VBORDER	Supply for border area, typically connect to VCOm via 10MΩ resistor
8	SPI_MISO	SPI MISO for EPDC host interface
9	VCC_3V3	3V3 power pin
10	SPI_MOSI	SPI MOSI for EPDC host interface
11	GD_SP	Gate start pulse
12	HRDY	Hardware ready
13	GD_CLK	Gate clock, connect to gate driver
14	GND	Ground
15	GD_OE	Gate output enable, connect to gate driver
16	SPICS	SPI chip select for EPDC host interface
17	VCOM	Switched VCOM supply (tuned for each panel)
18	MP_RESET	EPDC power-on reset pin
19	VME2	Power supply for EPDC internal PROM, currently not used, leave open
20	PWRSTAT	EPDC power status, currently not used, connect to VCC
21	VME1	Power supply for EPDC internal PROM, currently not used, leave open
22	PWRCOM	EPDC power control output, currently not used, leave open
23	GD_RL	Gate driver direction direction
24	PWR0	EPDC power control output, currently not used, leave open
25, 26	GND	Ground

Table 3: Electrical pin-out (source connector)

Pin number	Symbol	Function
1	GD_UD	EPDC clock, connect to 3V3.

Pin number	Symbol	Function
2	VCC_3V3	3V3 power pin
3	VGPOS	Positive HV supply for gate driver (+25V typ)
4	GD_SP	Gate start pulse
5	GND	Ground
6	GD_CLK	Gate clock
7	VGNEG	Negative HV supply for gate driver (-32V typ)
8	GD_OE	SPI MISO for EPDC host interface
9	GND	Ground
10	VCOM	Switched VCOM supply (tuned for each panel)

Table 6: Electrical pin-out (gate connector)

4.2 DC characteristics

Signal	Parameter	Min	Typ	Max	Unit
GND	Signal ground	-	0	-	V
VDD	Logic power supply	3.0	3.3	3.6	V
VGH	HV power supply for gate positive	23	25	27	V
VGL	HV power supply for gate negative	-34	-32	-30	V
VPOS	HV power supply for source positive	14.6	15	15.4	V
VNEG	HV power supply for source negative	-15.4	-15	-14.6	V
VASYM	Asymmetry source (VPOS+VNEG)	-150	0	150	mV
VCOM*	Common voltage	1	5.0	9	V

*VCOM will need to be tuned for each display module. The correct value will be supplied as part of the waveform data.

Table 4: DC characteristics

4.3 Controller

These displays use an EPSON S1D13541 EPD (Electrical Paper Display) source driver and controller. This chip integrates the source driver, EPD display engine, Display Memory, Waveform Memory, Command Memory, Multi Time PROM and temperature sensing system. In these displays the controller is combined with an UC8434 gate driver.

Key features:

- Serial Interface (SPI) as Host interface
- Transparency write

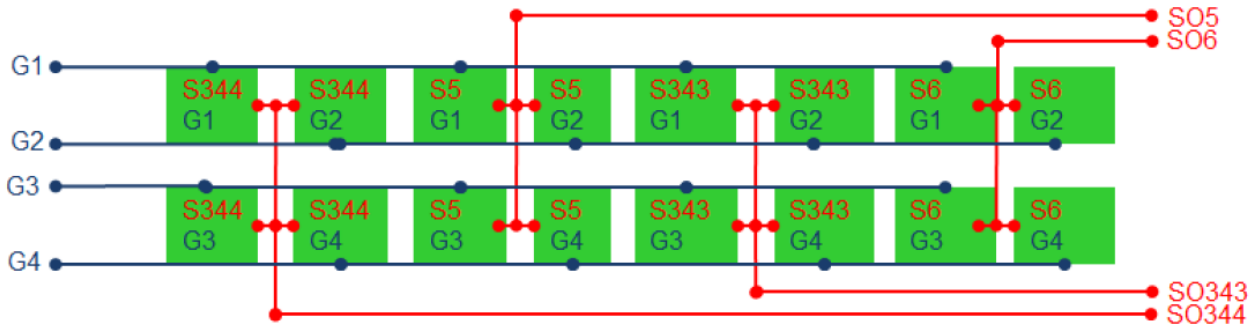
- Supported Data Formats: 1bpp, 2bpp, 4bpp, 1 Byte-per-pixel
- 202K Bytes Image Buffer
- Mirror and Rotate mode (Vertical/Horizontal Mirror, 0°/90°/180°/270° Rotate)
- 16K Bytes embedded memory for Waveform storage
- 16 or 32MHz clock input
- Built-in thermistor sensing system (external thermistor)
- I2C serial master
- External Gate driver control, Type 1
- External Power Management IC control

Please refer to EPSON S1D13541 datasheet for full controller specification.

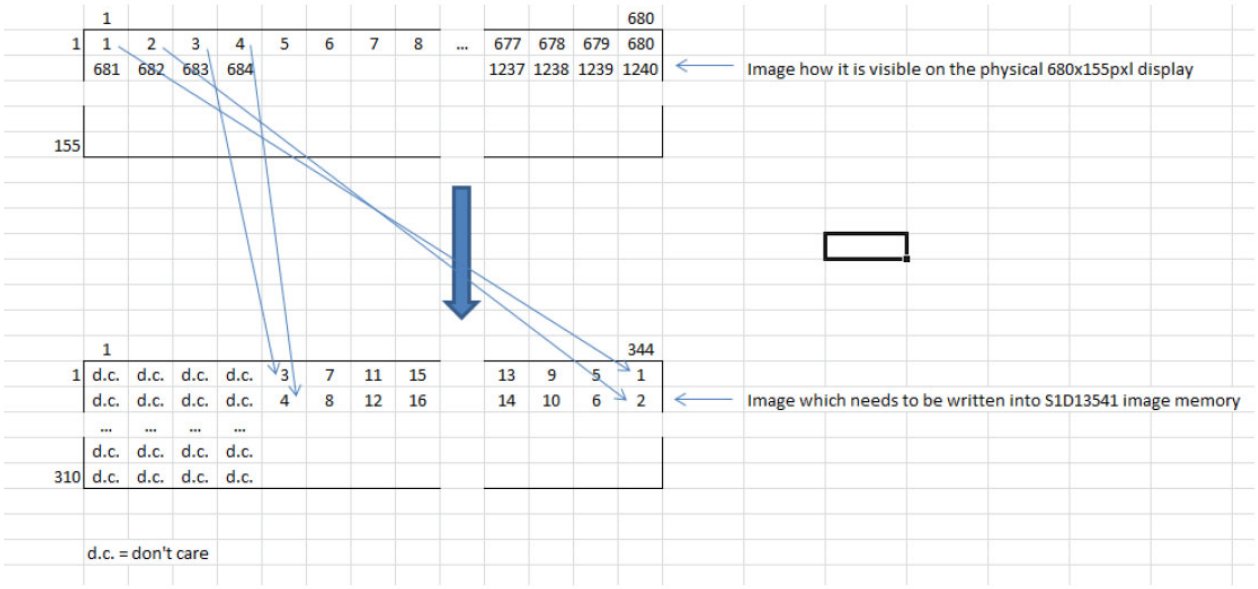
4.4 **"Scrambling"**

The display module does not have the physical source and gate lines 1:1 connected to the source and gate driver output lines. This is because:

- Line sharing is used
- Source lines are "interleaved"
- The source line driver only supports multiples of 8 → this results in four dummy source outputs



This configuration requires a "resorting" or "scrampling" of the image data. The data coming from a 680x155pxl image needs to get "scrambled" into a 344x310px image. This 344x310px image must be transferred into the Epson S1D13541 image memory in order to display the original 680x155pxl image.



4.5 Display Power Supply System

The display module itself does not contain the power management subsystem required to generate the high voltages driving the display. Reference circuitry can be provided by Plastic Logic recommending TI TPS65185.

5. Safety and Flammability requirements

The integrator of this display module into a final product is responsible for ensuring that the relevant safety and flammability requirements are met.

6. Compatible Evaluation Kits

Do not use any other than the recommended evaluation Kit.