PLASTIC LOGIC

Display Datasheet

3.1", 105 ppi,

312x74 pixels

Part-No. 700524

Type S031_T1.1

Revision 2

11-Sep-2018

![Plastic Logic logo]

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Revision Status	Date	Author	Reason of Modification
1	12-October-2017	RN	Initial Version copied from #700521 - Drawing including flex tail updated - Reference schematics updated - Pin assignment updated - Power consumption updated
2	02-Mar-2018 07-Jun-2018 11-Sep-2018	AF RN RN	- Format Update - Chapter re-arrangement & content update - Dimensions corrected - Reference schematics updated - Drawing updated - Power consumption updated

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Contents

1. Introduction

1.1 Purpose of this document

This document describes the technical specification of the Plastic Logic 3.1'' 312x74 pixel display module using the Ultrachip EPD controller/driver UC8156. It defines general characteristics of the display module and the technical information required to integrate the display module into a product.

1.2 Key features of display module

- Consists of an active matrix electrophoretic display which has an integrated EPD controller + source and gate driver IC bonded on the plastic substrate
- Display based on organic TFT active matrix
- 312 x 74 pixels @ 105 ppi equivalent to 242 μm pixel size
- 2 or 4 grey levels
- Incorporates industry-leading bi-stable electrophoretic display technology
- Ultra-wide viewing angle
- Enables robust product design
- Flexible
- SPI interface to customer application

1.3 Handling requirements

- Please assemble or install the displays in a clean working area.
- Take appropriate care to protect the rear side of the display module from indents and punctures as this may damage the display.
- The display module is an electrostatic discharge (ESD) sensitive device. Ensure proper ESD precautions are in place to avoid damage to the display module. Take care on grounding (e.g. wrist straps) maybe use ion fans.
- Please handle the display with care during assembly. Do not over-bend and twist the display. Protect especially the COP (chip on plastic) region.
- Do not connect or disconnect the display from the interface connector while power is on (no "hot-plugging").
- Do not stack the displays.

1.4 General parameters

Parameter	Value	Comments
Module dimensions	85.0 mm x 39.04 mm	Outer dimensions including display connector tail
Active screen dimensions	75.5 mm x 17.91 mm	Equivalent to 3.1 inch diagonal
Module thickness	0.48 mm +/- 0.05mm	Without liners

Parameter	Value	Comments
Active screen resolution	312 x 74 pixels	
Active screen pixel pitch	242 µm	Equivalent to approx. 105 ppi., square pixel
Bending radius (minimum)	30 mm	Active display area [1]
	40 mm	Chip area
Fully integrated EPD controller/driver	UC8156	Bonded on the plastic substrate (COP)
Surface treatment	Anti-glare, UV protection and hard coat (2H)	

[1] Cosmetical fold in black backencap (back side encapsulation material), AHS test still ok

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2. Mechanical specifications

FRONT(Flat)
(w/o Protective Liner)

Bottom(Flat)

DETAIL B
SCALE 5 : 1

BACK(Flat)

DETAIL A
SCALE 20 : 1

UNLESS OTHERWISE SPECIFIED: -DIMENSIONS ARE IN MILLIMETERS -ANGULAR TOLERANCES: ±0.5° -LINEAR TOLERANCES: ±0.2	PROPRIETARY AND CONFIDENTIAL THE INFORMATION CONTAINED IN THIS DRAWING IS THE SOLE PROPERTY OF PLASTIC LOGIC. ANY REPRODUCTION IN PART OR AS A WHOLE WITHOUT THE WRITTEN PERMISSION OF PLASTIC LOGIC IS PROHIBITED.	DEBUR AND BREAK SHARP EDGES	DO NOT SCALE DRAWING	REVISION 01F

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	NAME	DATE		NAME:
DRAWN BY	olka.kaveh	21.08.2018		**BW Display 3.1" 105ppi** **S031-B0074x0312** **P/N 700524**
		MATERIAL:		DRAWINGNR. DMO_700524_S031-B0074x0312
		WEIGHT:		SCALE: 1:1

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3. Optical specifications

3.1 Optical parameter

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Reflectance White	R_w	30	38 … 41		%
Contrast Ratio	CR	5:1	8:1 … 10:1		
Ghosting			<1	2	L*

Table 1: Optical parameter

Notes:

- The reflectance and contrast ratio is measured between 0ºC and 40°C at 50%rH.
- Reflectance measurements are done using a spectrophotometer. Plastic Logic is using the "spectro guide" from BYK-Gardner GmbH.
- L* is the lightness component of the CIE1976 CIELUV and CIELAB colour spaces. Measurements in L* can be related to reflectivity using the formula $L^*=116(L/L_w)^{1/3}-16$, where L and L_w are measured in % reflectance and L_w is defined as 100%. This formula is only valid for L*>16.
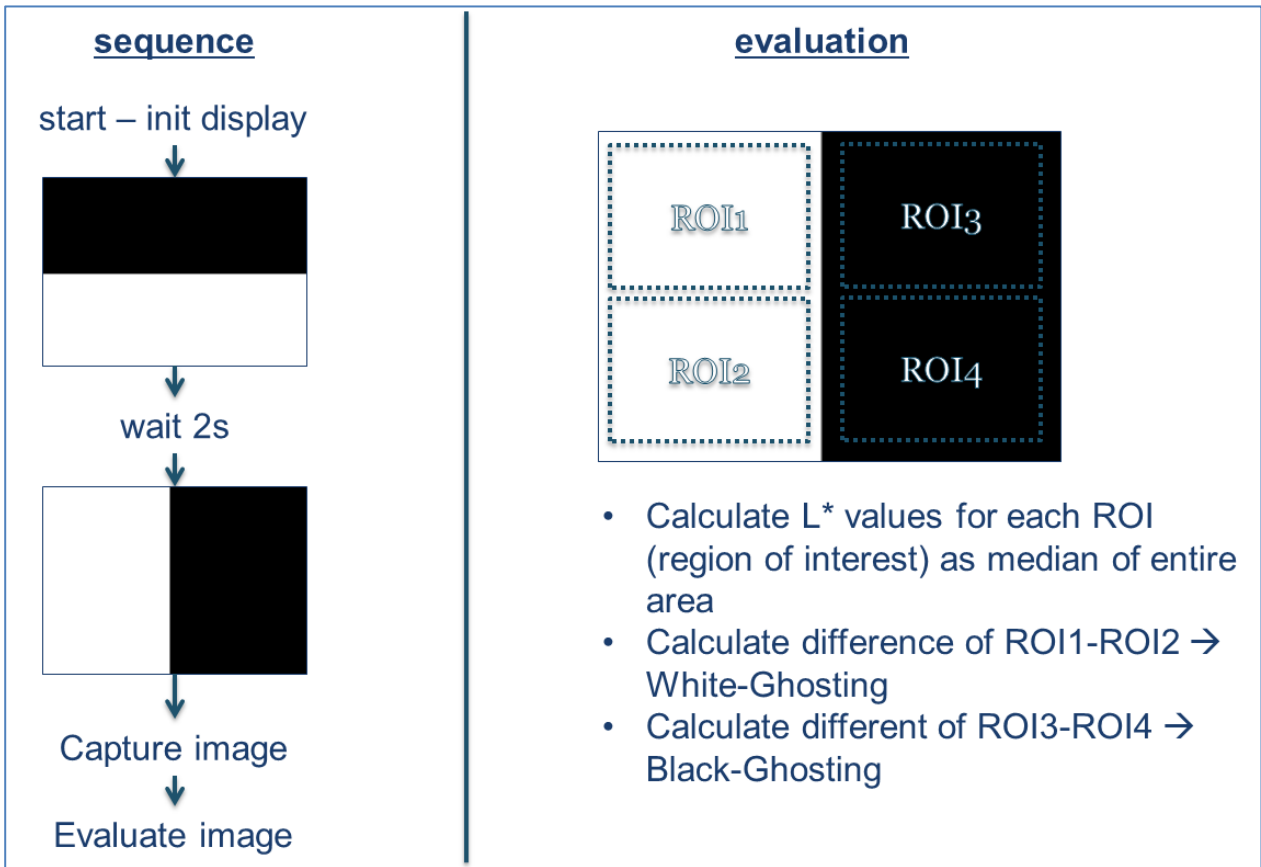
3.1.1 Ghosting measurement method

Figure 1 - ghosting measurement method

3.2 Waveform and update time

The update time is very much dependent on the waveform design. It might vary based on:

- Number of grey level (GL)
- Expected optical performance (contrast, ghosting, etc.).

Temp [°C]	>15	10-15	5-10	0-5
Typical update time [sec]	<0.9	<2.0	<2.5	<3.5

Note: "Update time" is complete BUSY high time

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4. Temperature Range and Humidity

Parameter	Value	Unit	Comments
Operating Temperature	0 to 40	degC	15%rH to 85%rH*
Storage Temperature Range	-25 to 50	degC	15%rH to 85%rH*

*Long-term exposure of stress close to limits might reduce overall lifetime

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5. Electrical specifications

5.1 Connector interface description

Displays are designed with a 26-pin connector on the flex tail.

Reference connector type: Omron XF2M-2615-1A, 26-pin Rotary Backlock Connector or Hirose FH34SRJ-26S-0.5SH(50), both dual contact, 0.5 mm pitch.

Pin number	Symbol	Purpose	Function
1,2	VSL	Output	Negative source voltage, connect to capacitor
3,4	VSH	Output	Positive source voltage, connect to capacitor
5,6	VGL	Input	Negative gate voltage, input from booster
7,8	VGH	Input	Positive gate voltage, input from booster
9	GDR_P	Output	P-MOS booster gate control
10	GDR_N	Output	N-MOS booster gate control
11	VDDIO	Power Supply	Interface power connect to VDDA for 3.3V I/O, connect to VDD for 1.8V I/O
12	VDDA	Power Supply	Analog power
13	SPI_MISO	Output	SPI data output
14	SPI_MOSI	Input	SPI data input
15	SPI_CLK	Input	SPI clock
16	SPI_CS	Input	SPI chip select
17	RST_N	Input	Global reset, low active When RST_N becomes low, driver will reset. All registers will be reset to default value and all driver functions will be disabled. SD output and VCOM will base on previous condition; they may have two conditions: 0V or floating.
18	BUSY_N	Output	BUSY pin - indicates the driver status. L: Controller / Driver is busy H: non-busy. Host side can send command/data to driver.
19	GND	Power Supply	Ground
20,21	VDD	Power Supply	Core Logic Power VDD can be regulated internally from VDDA. A capacitor should be connected between VDD and GND.
22	VDDA	Power Supply	Analog power
23	EXTVDD	Input	Controls internal regulator for VDD EXTVDD connected GND: internal regulator is on. EXTVDD connected VDDA: internal regulator is off, need an external 1.8V supply to VDD.
24,25	GND	Power Supply	Ground
26	TPCOM	Output	Connect to capacitor

Note: Refer to the display drawing for Pin1 location.

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5.2 Controller

The display is driven and controlled by the UC8156 which is an all-in-one EPD driver and timing controller from Ultrachip. This chip is bonded to the Plastic Logic display substrate using the "Chip on Plastic" (COP) technology.

Please refer to the Ultrachip UC8156 datasheet for the full controller specification.

5.3 Application reference circuit

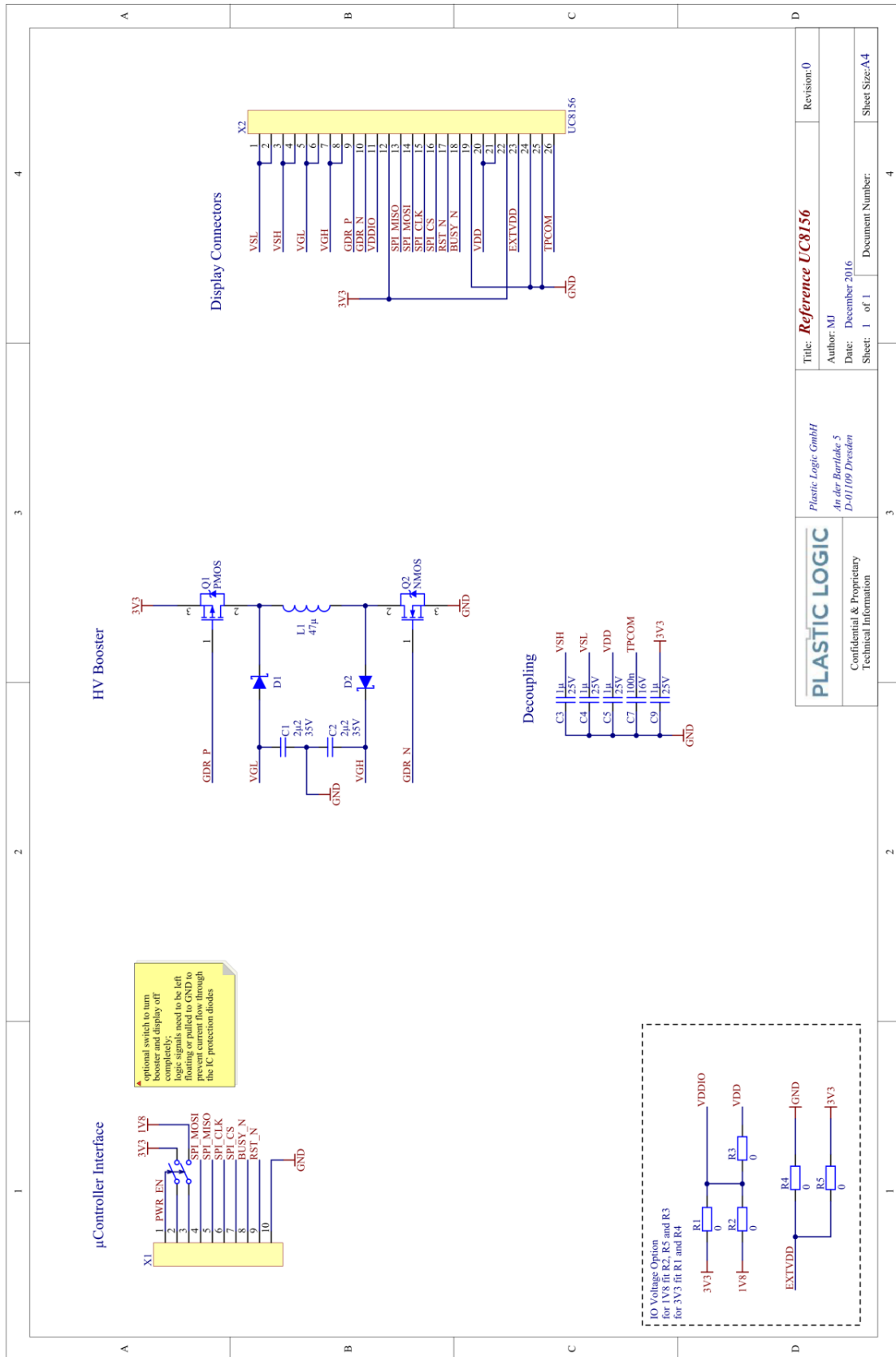**Figure 2 - Application reference circuit**

5.4 Display power consumption

Mode	Parameter	Typical	Maximum	Unit
Operation	Mean current for "typical" image update	6		mA
Operation	Mean current for a "worst case" image update	12		mA
Operation	Peak current	160	300	mA
Stand-by with HV's on	Stand-by current 1	4		mA
Stand-by with HV's off	Stand-by current 2	30		µA
Sleep	Sleep current	0.7	0.8	µA

Note (1):   see detailed conditions, measurement setup and value calculation below

Note (2):   peak current duration ~ 10 µs

Power consumption is very much depending on the finally implemented waveform.

5.4.1 Conditions

1) "Worst case" image = stripe pattern to inverse stripe pattern

Figure 3 – "Worst case" image used for power consumption measurement

horizontal 4-

2) "Typical" image =
grey scale to vertical 4-grey scale

Figure 4 – "Typical" image used for power consumption measurement

3) Room temperature conditions (ca. 23°C + 50%rH)
4) Latest register settings and operation sequence used. Waveform and VCOM value is already programmed into controller internal memory.

5.4.2 Measurement setup

Power consumption specifications were determined by utilizing high side current measurements on the supply power line of the displays. The current rating was detected by measuring the voltage drop over a 0.01 Ohm shunt resistor applying a burden voltage of 10 μ V/mA to the display and sub-sequentially amplifying the signal with an ultra-low offset/drift, low noise precision amplifier. The amplified signal was either detected by an oscilloscope sampling the signal with 2.5 MS/s or a digital multimeter.
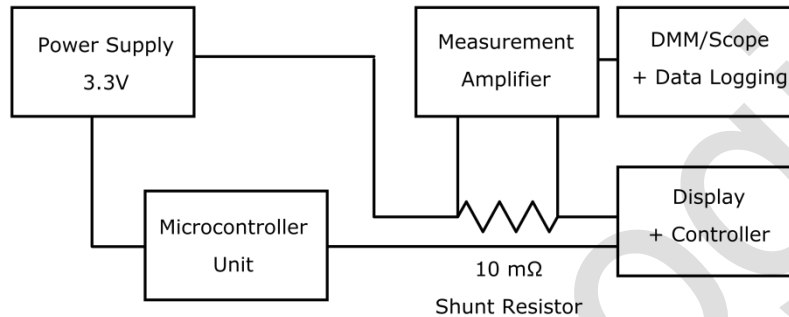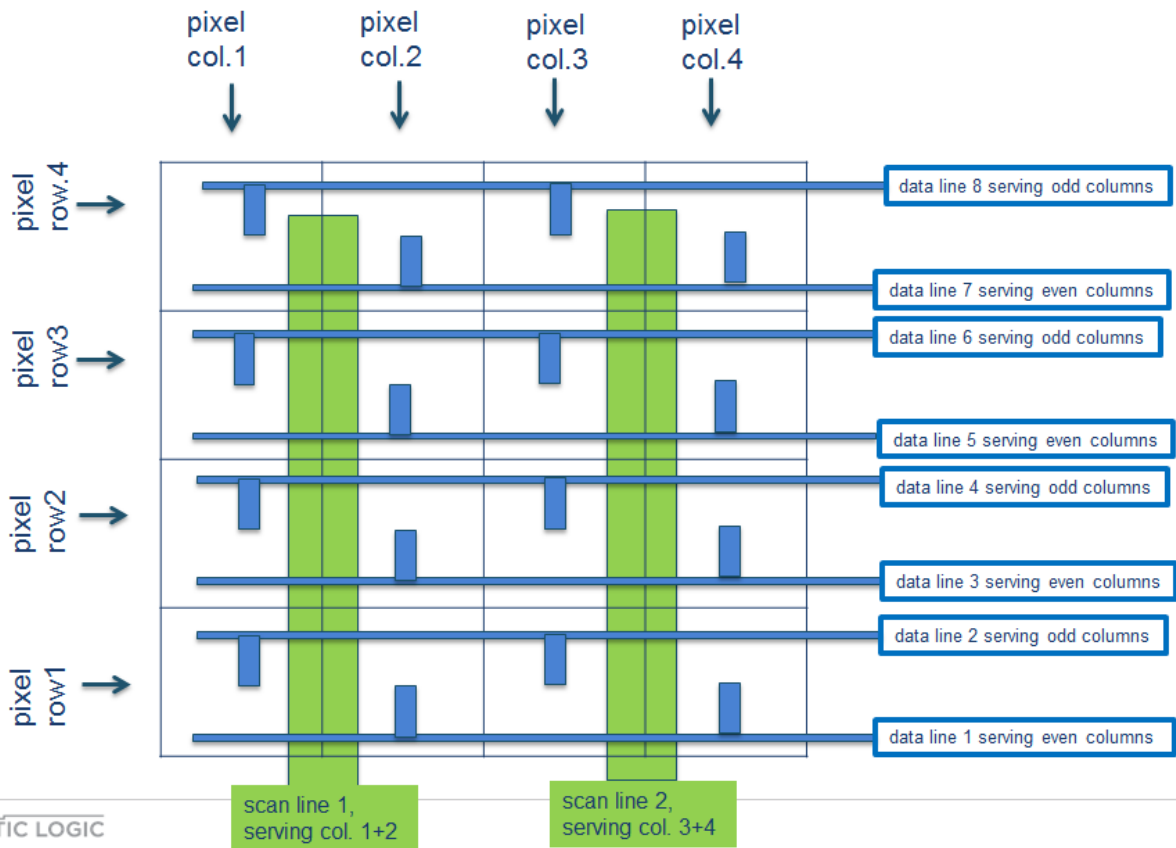

Figure 5 - Measurement Setup

5.4.3 Value calculation for mean power

- The "input current" value is calculated as <u>average</u> value over the whole update (approx. BUSY high time).
- The given value includes the consumption of the display and the complete external display related electronic (HV generation).

5.5 Scrambling

Scrambling is used to share the gate lines between 2 pixels but requires 2 physical source lines per source row. The scrambling converts 148x156 physical lines into the virtual resolution of 74x312 pixel. Picture content to be shown on the display has to be converted according to this scrambling before sending it to the display. Example source code for implementing this functionality is provided with the evaluation kit.

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The following sketch shows how scrambling works in detail:

6. Safety and Flammability requirements

The integrator of this display module into a final product is responsible for ensuring that the relevant safety and flammability requirements are met.

7. Compatible Evaluation Kits

Do not use any other than the recommended evaluation Kit.